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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,319	01/30/2002	Chuichi Miyazaki	501.35286C14	7381

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ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

EXAMINER

THAI, LUAN C

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 08/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/058,319

Applicant(s)

MIYAZAKI ET AL.

Examiner

Luan Thai

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 15-17 is/are rejected.
- 7) ☒ Claim(s) 14 and 18-20 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 & 3 1/2 6) ☐ Other: ____

DETAILED ACTION

Priority

1. This application is a continuation of U.S. Application Serial Number 09/768,451, filed January 25, 2001, and now U.S. Patent Number 6,355,500.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5-9, 11-13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Distefano et al (5,776,796) in view of Ghoshal et al (5,863,970).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-3, 5-9, and 11-13, Distefano et al (see specifically figures 6A-6G and 7A-7G) disclose a method of manufacturing a semiconductor device comprising the steps of:

(a) providing a semiconductor chip 12 having a plurality of external terminals 24' formed on a main surface thereof (although XXX does not explicitly teach a plurality of semiconductor elements formed on the main surface of the chip, these features are taken to be inherent in the semiconductor chip YYY);

(b) providing a wiring substrate 14 comprising a polyimide tape 16 and a plurality of wirings 26 and an opening 50', the wirings are revealing on a main

surface of the wiring substrate and an encapsulant of epoxy-based resin 40 appended on a rear surface of the wiring substrate, opposite of the main surface thereof;

(c) adhering the main surface of the semiconductor chip on the rear surface of the wiring substrate by way of the epoxy-based resin 40 as the epoxy-based resin 40 is protruding from an outer periphery of the semiconductor chip 12;

(d) electrically connecting the plurality of wirings with the plurality of external terminals through the opening 50', respectively;

(d') forming a solder ball 46 on each of revealed portions of the wirings;

(e) after the step (d), cutting (along a same cutting line) the wiring substrate together with the epoxy-based resin 40 to form an outer periphery thereof outside of the outer periphery of the semiconductor chip (see figure 6G and 7G).

Although Distefano et al do not explicitly disclose the epoxy-based resin 40 being an adhesive as claimed, a epoxy-based resin is well known to be an adhesive material as disclosed by Ghoshal et al, Col. 2, lines 50+. Thus, it would have been obvious to consider the epoxy-based resin 40 in Distefano et al's structure as the claimed adhesive.

Regarding claim 15, Distefano et al disclose the layer 40 having a thickness larger than that of the wiring substrate 14.

The further citations of claims 16-17 would have been obvious for the similar reasons set forth in the discussion of claims 12-13, respectively.

4. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Distefano et al (5,776,796) in view of Ghoshal et al (5,863,970) and further in view of Nakamura et al (5,777,391 provided by Applicant).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 4 and 10, the proposed process of Distefano et al and Ghoshal et al discloses all the limitations of the claimed invention as detailed above except for gold wires being used for making electrical connection between the wirings of the wiring substrate and the external terminals of the chip (the proposed process of Distefano et al and Ghoshal et al teaching that connection being made through leads).

Nakamura et al while related to a similar process of manufacturing a semiconductor device teach gold wires being used for making electrical connection between the wirings of the wiring substrate and the external terminals of the chip (Col. 7, lines 37+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use gold wires to connect the wirings of the wiring substrate to the external terminals of the chip in order to improve the electrical connection between the chip and the wiring substrate.

Allowable Subject Matter

5. Claims 14 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance: none of the prior art of record whether taken singularly or in combination fails to anticipate or fairly suggest that which the Applicant claims in claims 14 and 18, especially when these limitations are considered within the specific combination claimed, to teach that the layer having adhesion is applied on the rear surface of the wiring substrate by printing.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
August 13, 2002

Albert W. Paladini 8-22-02
ALBERT W. PALADINI
PRIMARY EXAMINER